ABSTRACT

A digital crossbar switch utilizes an asynchronous RAM to provide high density and low latency storage and a write enable pulse generator to generate write enable pulses that are independent of the clock signal duty cycles. The crossbar switch includes a plurality of ports coupled to a bus, at least one memory element coupled to one of the plurality of ports, and a circuit for generating a write enable pulse coupled to each of the memory element. The circuit for generating the write enable pulse includes a pulse generator for generating a pulse, the pulse tracking a leading edge of a clock signal, a write enable signal generator for generating a write enable signal, and a first logic circuit coupled to the pulse generator and the write enable signal generator for generating the write enable pulse by combining the pulse and the write enable signal.